32x32 FERRITE CORE MEMORY SUBSYSTEM (COINCIDENT-CURRENT MATRIX & SENSE AMPLIFIER)

32x32 FERRITE CORE PLANE (1,024 BITS)

Hand-Woven Toroidal Core Matrix

Physical 4-Wire System

1. X-Drive Wire: Half-select drive current (Im / 2 = 190 mA)
2. Y-Drive Wire: Half-select drive current (Im / 2 = 190 mA)
3. Sense Wire: Threaded diagonally through all 1,024 cores
4. Inhibit Wire: Cancels write current when storing '0'

Magnetic Coercivity Hc: Remanence Endures Indefinitely!

100% Non-Volatile: Retains memory state with zero power

EMP & radiation immune (Aerospace & Industrial Grade)

Core Material: Lithium-Ferrite (T-50/12)

Destructive Read & Automatic Rewrite Cycle

1. READ Phase: Core is driven towards '0'

→ If core was '1': Induction pulse generated on Sense wire

2. WRITE Phase: Original state immediately restored

Full Cycle Time (Read + Restore): 1.2 µs

Automatic hardware refresh executed on Baseboard

X/Y DRIVERS & INHIBIT STAGE

Constant-Current Half-Select Drivers

Discrete Constant-Current Sources (190 mA)

4x 32-Pin driver sockets for X and Y axes

74HC138 decoders switch discrete H-bridge stages

Direction reversal for Read vs Write current pulses

Ultra-Steep Edges (< 20 ns) for Pristine Induction

Inhibit Driver Stages

Counter-current through inhibit winding

Cancels write current when data bit is '0'

1N5819 Schottky Diodes for Spark Quenching

ZIF-40 Socket for swappable memory cartridges

12x HDSP-7803 Green 7-Segment Displays

Controller Baseboard (Board 02)

Zero-DRC / Zero-ERC Release for JLCPCB

SENSE AMPLIFIER & DISCRIMINATOR

Differential Sense Wire Detection

LM311 / NE521 High-Speed Comparator

Induction signal: Only 15 to 40 mV amplitude!

Balanced differential input cancels common-mode noise

Threshold setting via precision multi-turn trimmer

Reliable discrimination between '1' and '0'

Strobe Window Integrator

Samples sense voltage strictly inside peak window

Blanks out capacitive switching transients

Output strobes 74HCT574 Data Bus Latch

Zero-Wait-State transfer to CLACK-BUS

Bus Interface: 40-Pin CLACK-BUS J_CLACK_STACK

Full historical & functional authenticity

Christian Buchhas • Antigravity • Ref: Peter Prikasky

16-BIT DATA BUS (D0..D15) & CORE TIMING SIGNALS (STROBE, READ, REWRITE)

16-BIT RELAY MAINFRAME (CLACK-MAINFRAME) **32x32 FERRITE CORE MEMORY SUBSYSTEM**			
Architecture & Hardware Engineering: **Christian Buchhas • Antigravity** Original CPU Concept: Peter Prikasky (relaiscomputer.at)		Document No.: **CLACK-MEM-01**	
Standard & Specification: **Eurocard 3U • 40-Pin CLACK-BUS • relaycomputer.org**		Date: **2026-11-04**	Rev / Sheet: **v2.0 (1 / 1)**