DATA BUS (16-BIT)

16

16-Bit Bi-Direct

IR
16-BIT
Instruction Register

Temp Step Register
4-BIT
Intermediate Step Buffer

FEEDBACK: next Step

Accu
16-BIT
Accumulator Register

Direct Addr

16

AR
16-BIT
Address Register

Drive Addr

16 (10)

Opcode [15:10] & Address Type

Clock Transfer

Operand A (Accu)

Instruction Decoder
DECODER
6-to-64 Command Decoder

Step Register
4-BIT
Active Microstep Latch

ALU
ARITHMETIC
16-Bit Manchester Carry Unit

Operand B (Bus)

PC_HR
16-BIT
PC Buffer Register

Command Lines (64)

Step Decoder
DECODER
4-to-16 Microstep Decoder

+1
FAST INC
Relay Incrementer (Add 1)

PC Feedback to PC_HR

ALU Result [15:0]

Step Lines (16)

PC + 1

Accu ER
16-BIT
ALU Result Register (Latch)

Tri-State Output

Branch Load

PC
16-BIT
Program Counter Register

Fetch Addr

DIODE & RELAY CONTROL MATRIX (COMMAND & STEP MATRIX)

&

&

&

next Step

ControlLines

SR
16-BIT
Stack / Subroutine Register

Call / Return Link

AB-R
BUS DRIVE
Address Bus Driver Register

ADDRESS BUS (A0..A15)

DATA BUS (16-BIT D0..D15)

Control Lines

Clock 0..3 (T0..T3)

Control Line Timing
TIMING
4-Phase Non-Overlapping Gate

OE, IE, Rd, WR, MUX, ALU_OP

16-BIT RELAY MAINFRAME (CLACK-MAINFRAME)

LOGIC ARCHITECTURE & CPU DATA PATH

Architecture & Hardware Engineering: **Christian Buchhas • Antigravity** Original CPU Concept: Peter Prikasky (relaiscomputer.at)	Document No.: **CLACK-LOGIC-01**	
Standard & Specification: **Eurocard 3U • 40-Pin CLACK-BUS • relaycomputer.org**	Date: **2026-11-04**	Rev / Sheet: **v2.0 (1 / 1)**