POD 01: 16-BIT HIGH-SPEED MANCHESTER ALU & CARRY CHAIN LOGIC

OPERAND INPUTS: ACCU (OP-A [15:0]) & DATA BUS (OP-B [15:0])

BIT-SLICE 0 (LSB)

Logic Functions (AND, OR, XOR, NOT)

Pi = Ai XOR Bi (Propagate Condition)

Gi = Ai AND Bi (Generate Condition)

Ki = NOT Ai AND NOT Bi (Kill Condition)

Relay Contacts: 2x HKE SIP-1A05 (0% ICs)

Manchester Carry Bypass Switch

When Pi = 1: C_out = C_in (Pass-Through)

When Gi = 1: C_out = +5V (Generate Carry)

When Ki = 1: C_out = GND (Absorb Carry)

Bypass Delay: < 2ns per Bit Stage!

Sum Generation & Relay Latch

Si = Pi XOR C_in

Relay contacts drive result bus

Result Bit: D_out[i]

BIT-SLICE 1

Logic Functions (AND, OR, XOR, NOT)

Pi = Ai XOR Bi (Propagate Condition)

Gi = Ai AND Bi (Generate Condition)

Ki = NOT Ai AND NOT Bi (Kill Condition)

Relay Contacts: 2x HKE SIP-1A05 (0% ICs)

Manchester Carry Bypass Switch

When Pi = 1: C_out = C_in (Pass-Through)

When Gi = 1: C_out = +5V (Generate Carry)

When Ki = 1: C_out = GND (Abs

Bypass Delay: < 2ns per Bit Stage!

Sum Generation & Relay Latch

Si = Pi XOR C_in

Relay contacts drive result bus

Result Bit: D_out[i]

BIT-SLICE 2

Logic Functions (AND, OR, XOR, NOT)

Pi = Ai XOR Bi (Propagate Condition)

Gi = Ai AND Bi (Generate Condition)

Ki = NOT Ai AND NOT Bi (Kill Condition)

Relay Contacts: 2x HKE SIP-1A05 (0% ICs)

Manchester Carry Bypass Switch

When Pi = 1: C_out = C_in (Pass-Through)

When Gi = 1: C_out = +5V (Generate Carry)

ID (Absorb Carry)

Bypass Delay: < 2ns per Bit Stage!

Sum Generation & Relay Latch

Si = Pi XOR C_in

Relay contacts drive result bus

Result Bit: D_out[i]

BIT-SLICE 15 (MSB)

Logic Functions (AND, OR, XOR, NOT)

Pi = Ai XOR Bi (Propagate Condition)

Gi = Ai AND Bi (Generate Condition)

Ki = NOT Ai AND NOT Bi (Kill Condition)

Relay Contacts: 2x HKE SIP-1A05 (0% ICs)

Manchester Carry Bypass Switch

When Pi = 1: C_out = C_in (Pass-Through)

When Gi = 1: C_out = +5V (Generate Carry)

When Ki = 1: C_out = GND (Absorb Carry)

Bypass Delay: < 2ns per Bit Stage!

Sum Generation & Relay Latch

Si = Pi XOR C_in

Relay contacts drive result bus

Result Bit: D_out[i]

HIGH-SPEED CARRY RAIL (SUB-2ns MANCHESTER BYPASS)

ALU STATUS FLAGS (C, Z, N, V)

CARRY FLAG (C)

Carry out of Bit 15

C = C_out[15]

ZERO FLAG (Z)

NOR Gate across D0..D15

Z = 1 when Result == 0

NEGATIVE FLAG (N)

Sign Bit 15

N = Result[15]

OVERFLOW FLAG (V)

Two's Complement Overflow

V = C_in[15] XOR C_out[15]

16-BIT RELAY MAINFRAME (CLACK-MAINFRAME)

POD 01: 16-BIT MANCHESTER ALU LOGIC

Architecture & Hardware Engineering:
Christian Buchhas • Antigravity
Original CPU Concept: Peter Prikasky (relaiscomputer.at)

Document No.:
CLACK-POD-01

Standard & Specification:
Eurocard 3U • 40-Pin CLACK-BUS • relaycomputer.org

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