POD 02: 16-BIT DUAL-PORT REGISTER FILE & REED-RELAY BUS ISOLATION

ACC
Accumulator
Primary Math Register

16x HKE SIP-1A05 Self-Holding Relays
16-Bit Storage Depth (0% ICs)

4x HKE SIP-1A05 Reed Relays
Galvanic Bus Isolation

R0
General Register 0
Data & Address Pointer

16x HKE SIP-1A05 Self-Holding Relays
16-Bit Storage Depth (0% ICs)

4x HKE SIP-1A05 Reed Relays
Galvanic Bus Isolation

R1
General Register 1
Counter & Loop Index

16x HKE SIP-1A05 Self-Holding Relays
16-Bit Storage Depth (0% ICs)

4x HKE SIP-1A05 Reed Relays
Galvanic Bus Isolation

R2
General Register 2
Base Offset Pointer

16x HKE SIP-1A05 Self-Holding Relays
16-Bit Storage Depth (0% ICs)

4x HKE SIP-1A05 Reed Relays
Galvanic Bus Isolation

R3
General Register 3
Stack Helper Register

16x HKE SIP-1A05 Self-Holding Relays
16-Bit Storage Depth (0% ICs)

4x HKE SIP-1A05 Reed Relays
Galvanic Bus Isolation

TMP
Temporary Register
ALU Latch Buffer

16x HKE SIP-1A05 Self-Holding Relays
16-Bit Storage Depth (0% ICs)

4x HKE SIP-1A05 Reed Relays
Galvanic Bus Isolation

CONTROL & ADDRESS DECODING (100% RELAYS & DIODES)

Diode Matrix 3-to-8 Decoder (100% Pure Relays & Diodes)

RegSel[2:0] = 000 → ACC Enable
RegSel[2:0] = 001..100 → R0..R3 Enable
RegSel[2:0] = 101 → TMP Enable

Diode matrix drives register coils directly (0% ICs)

Dual-Port Read and Write Paths

Port A (Read): Galvanic isolation via reed relay contacts
Port B (Write): Latch-enable pulse from control sequencer

Zero-Wait-State Register Transfer in 1 Clock Cycle

Integrated 16x 3mm LED Status Display (Frontpanel)

Series Resistors: 330 Ohm Metal Film 1%

Bus Interface: 40-Pin CLACK-BUS J_CLACK_STACK

16-BIT DATA BUS INTERFACE (D0..D15) & RELAY DRIVERS

16-BIT RELAY MAINFRAME (CLACK-MAINFRAME)
POD 02: 16-BIT REGISTER FILE LOGIC

Architecture & Hardware Engineering: **Christian Buchhas • Antigravity** Original CPU Concept: Peter Prikasky (relaiscomputer.at)	Document No.: **CLACK-POD-02**	
Standard & Specification: **Eurocard 3U • 40-Pin CLACK-BUS • relaycomputer.org**	Date: **2026-11-04**	Rev / Sheet: **v2.0 (1 / 1)**