POD 04: 4-PHASE CLOCK GENERATOR, DIODE MATRIX MICROCODE & 10V OVERDRIVE PULSE SHAPER

4-PHASE MASTER CLOCK

Non-Overlapping Phase Generator

Relay Ring Counter & 4-Phase Sequencer

Adjustable Frequency: 1 Hz (Single-Step) to 1,500 Hz

Phases: T0 (Fetch), T1 (Decode), T2 (Execute), T3 (Writeback)

Dead Time: 50µs between phases for spark suppression

Guarantees 100% Contact-Bounce-Free Switching

Clock Waveform & Timing Budget

T0: Fetch instruction from ROM/RAM → Load IR (150µs)

T1: Diode matrix decodes opcode → Fetch operands (200µs)

T2: ALU Manchester carry operation (180µs)

T3: Writeback result to Register / Core RAM (220µs)

Total Cycle Time: 1,000 µs → 1,000 IPS Peak!

Status LEDs: T0, T1, T2, T3 (Green/Amber)

RUN / HALT / SINGLE-STEP Switch Inputs

100% THT Zero-Defect Design

10V/2.5V OVERDRIVE PULSE SHAPER

Dynamic Relay Coil Driver

Two-Tier Relay Energization Profile

1. Pull-in Pulse (80µs): 10V Overdrive

→ Closes reed relay in 0.25 ms (4x faster!)

2. Hold Voltage: Drops down to 2.5V

Reduces Coil Power Dissipation by 75%!

Driver Stage & Protection Circuitry

Discrete BD139 / 2N3904 Transistor Drivers

Ultra-Fast 1N5819 Schottky Clamp Diodes

RC Snubbers for total spark quenching

Lifespan: > 1 Billion Switching Cycles

Automatic power-down on HALT state

Thermal stability: zero overheating risk

Zero-Defect Sign-off for 4-Core Mainframe

DIODE MATRIX MICROCODE ROM

Discrete Instruction Decoder (0% ICs)

32x 1N4148 Diodes in DIP Sockets

Every instruction can be modified in the field

by simply repositioning diodes — pure hardware logic!

Matrix Capacity: 64 Instructions x 16 Control Lines

No Firmware Flash Needed • Pure Physics

Supported 16-Bit Instruction Set

- LOAD / STORE: Memory & register transfers
- ADD, SUB, AND, OR, XOR, NOT, SHL, SHR
- ADDM [M], Reg (Direct memory addition)
- JMP, JZ, JNZ, JC, JNC, JN, JV (Conditional jumps)
- CALL, RET, PUSH, POP, NOP, HALT

Extendable with Coprocessor Opcodes (MUL, DIV)

Bus Interface: 40-Pin CLACK-BUS J_CLACK_STACK

MASTER CONTROL BUS (RW_n, STROBE, READY_WAIT, RESET_n) & PHASE OUTPUTS

16-BIT RELAY MAINFRAME (CLACK-MAINFRAME)

POD 04: SEQUENCER & PULSE DRIVER LOGIC

Architecture & Hardware Engineering: **Christian Buchhas • Antigravity** Original CPU Concept: Peter Prikasky (relaiscomputer.at)	Document No.: **CLACK-POD-04**	
Standard & Specification: **Eurocard 3U • 40-Pin CLACK-BUS • relaycomputer.org**	Date: **2026-11-04**	Rev / Sheet: **v2.0 (1 / 1)**