POD 07: 16-BIT HIGH-SPEED MATH COPROCESSOR (HARDWARE MULTIPLIER & BARREL SHIFTER)

16x16 HARDWARE MULTIPLIER

Booth / Wallace-Tree Acceleration Pipeline

Multiplication Array (MUL & IMUL)

Inputs: Multiplicand A [15:0] & Multiplier B [15:0]

Output: 32-Bit full product in (DX:AX)

Partial product reduction in 4 clock cycles

16x Hardware Speedup over Software Routines!

Hardware Divider (DIV & IDIV)

Non-restoring division algorithm

32-Bit dividend by 16-Bit divisor

Generates Quotient (AX) and Remainder (DX)

Hardware Division-by-Zero Exception

Relay Matrix: HKE SIP-1A05 & DIP-1C05

100% THT Construction • Eurocard 3U

Zero-Defect Release • 0 DRC Violations

16-BIT BARREL SHIFTER

Single-Cycle Shift & Rotate Unit

Logical & Arithmetic Shifts

SHL / SAL: Shift Left (Multiply by 2^n)

SHR: Logical Shift Right (Divide by 2^n)

SAR: Arithmetic Shift Right (Sign-Preserving)

Arbitrary Shift Distance 0..15 in 1 Clock Cycle!

Rotations (ROL, ROR, RCL, RCR)

Circular bit rotation with or without Carry Flag

Essential for cryptographic routines & bit manipulation

4-Stage Multiplexer Network (74HCT157 / 74HCT151)

Stage 1: 1-Bit • Stage 2: 2-Bit

Stage 3: 4-Bit • Stage 4: 8-Bit

Ultra-Low Propagation Delay (< 15 ns)

COPROCESSOR INTERFACE & I/O

Hardware Handshake & Registers

Command & Status Registers

MATH_CMD: Initiates computation cycle

MATH_STATUS: BUSY, DONE, OVERFLOW, DIV_BY_ZERO

READY_WAIT signal pauses CPU during division

Transparent instruction execution in assembly

Electrical Specification

Supply: +5V_MAIN (Pin 37) • GND (Pin 40)

Current consumption during multiplication: approx. 650 mA

4-Layer PCB with continuous ground plane

A*-Routing: 0 DRC violations, 0 unrouted pads

Bus Interface: 40-Pin CLACK-BUS J_CLACK_STACK

Full production release for 4-Core Mainframe

16-BIT DATA BUS (D0..D15) & COPROCESSOR COMMAND INTERFACE

16-BIT RELAY MAINFRAME (CLACK-MAINFRAME) **POD 07: MATH COPROCESSOR LOGIC**			
Architecture & Hardware Engineering: **Christian Buchhas • Antigravity** Original CPU Concept: Peter Prikasky (relaiscomputer.at)		Document No.: **CLACK-POD-07**	
Standard & Specification: **Eurocard 3U • 40-Pin CLACK-BUS • relaycomputer.org**		Date: **2026-11-04**	Rev / Sheet: **v2.0 (1 / 1)**